IN THE SPECIFICATION

Please replace the following paragraphs:

Page 1, Paragraph [0001].

[0001] The disclosures herein relate generally to information handling systems (IHS's) and more particularly to ~~techniques for~~ reducing the number of different types of connectors employed to support different devices in information handling systems.

Page 2, Paragraph [0003].

[0003] Many IHS's include a main board or motherboard in which several expansion connectors are situated on a common bus, for example, the Peripheral Component Interconnect (PCI) bus and the more recent PCI Express (PCIE) bus. Each expansion connector is capable of receiving an expansion card to provide additional capability to the system. Expansion cards are also known as add-in-cards (AICs).

Page 2, Paragraph [0004].

[0004] In additional to these standard PCI or PCIE bus connectors, a modern IHS is likely to include several other different and unique connectors especially as more and more functionally is integrated on motherboards. Contemporary IHS's often implement functions in software, for example, audio processing, or custom hardware, for example LAN MAC. In both cases, the physical layer is generally in a separate semiconductor device due to semiconductor process and cost considerations. Frequently, these functions interface to unique physical interconnect layers. For example, the LAN function interfaces through a Media Independent

audio function interfaces through an AC97 physical layer. Each of these interfaces is unique. The use of such multiple interfaces within the IHS is a significant factor in the current proliferation of multiple different unique connectors in the IHS. For example, AMR connectors are used to support "Audio Modem Riser" cards and CMR connectors are used to support "Communication Modem Riser" cards. Each of these connectors is different from the other and is also different from the PCI or PCIE connectors used for AICs in IHSs.

Page 4, Paragraph [0008].

[0008] FIG. 1A is a block diagram of an embodiment of an add-in-card (AIC) including a PCIE device.

Page 4, Paragraph [0009].

[0009] FIG. 1B is a block diagram of an embodiment of an AIC including a non-PCIE device

Page 4, Paragraph [0010].

[0010] FIG. 1C is a block diagram of another embodiment of an AIC including a non-PCIE device.

Page 4, Paragraph [0011].

[0011] FIG. 2 is a block diagram an embodiment of an information handling system employing the disclosed IHS.

Page 4, Paragraph [0012].

[0012] FIG. 3A – 3C are block diagrams of three embodiments of non-PCIE type AICs.

Page 4, Paragraph [0015].

[0015] FIG. 6A is a flow chart depicting an embodiment of the AIC type detection process carried out by the IHS.

Page 4, Paragraph [0016].

[0016] FIG. 6B is a flow chart depicting an embodiment of the process of configuring the IHS for supporting a non PCIE type AIC which calls for a programmable integrated function.

Page 6, Paragraph [0023].

[0023] Host bridge 210 includes a PCIE output which is coupled to a PCIE link or bus 230. PCIE link 230 is coupled to I/O hub 240 which includes a plurality of like PCIE outputs 235 which are also designated as PCIE connectors PCIECONN1, PCIECONN2, ... PCIECONN-N wherein N is the maximum number of AICs which the particular IHS 200 is to accommodate at one time in N respective connectors. These PCIE connectors are all designated as PCIE connectors 235 ~~since~~ because they are substantially the same type of industry standard connector. Any one of PCIE connectors 235 can receive any one of AICs 100, 120 and 140 of FIG.'s 1A – 1C therein whether the respective card includes a PCIE device or a non-PCIE device. For discussion purposes it assumed that a PCIE device AIC 100 is connected to PCIECONN1 and that non PCIE device AICs 120 and 140 are connected to PCIECONN2 and PCIECONN-N. In this example, there are 3

PCIECONN connectors such that N = 3. The disclosed technology can accommodate a larger number of connectors and AICs as well.

Page 8, Paragraph [0027].

[0027] In this particular example, INTEGRATED FUNCTION A is an audio function and INTEGRATED FUNCTION A sends audio information received from PCIE link 230 across SWITCH2 to packet interface A' which acts as a protocol translator to packetize the audio information. The packetized audio information is sent via MUX2 and connector PCIECONN2 to non PCIE AIC 120 for additional handling.

Page 8, Paragraph [0028].

[0028] In one embodiment, a physical layer 255, such as an audio physical layer, is situated on a motherboard 260 in IHS 200. Physical layer 255 is coupled to INTEGRATED FUNCTION A packet interface A' as shown. ~~(You could take over or not take over – so just remove this sentence as we have done already - but just leave with the correction)~~ AIC2 works in conjunction with INTEGRATED FUNCTION A to provide audio functionality. It is noted that PACKET INTERFACE A of AIC 120 cooperates with PACKET INTERFACE A' to transfer audio information back and forth between PCIE link 230 and AIC 120. When PACKET INTERFACE A' acts as a packetizer, PACKET INTERFACE A of AIC 120 acts as a de-packetizer, and vice versa. Physical layer 255 is an AC'97 compatible codec in one embodiment of IHS 200.

Pages 11 through 12, Paragraph [0035].

[0035] FIG. 5 is a flowchart depicting the operation of IHS 400. Operation commences as per block 500 when the power button of the system is pressed or reset. It will be recalled that IHS 400 includes one fixed integrated function 251 and

one programmable integrated function 402. Each of these functions can accommodate one corresponding AIC. Thus, an error condition exists if there is more than one AIC installed which calls for a fixed integrated function. A test is conducted at decision block 505 to determine if more than one AIC calling for a fixed integrated function has been detected. If so, an error condition exists as per block 510 and processing halts as per end block 515. In this particular embodiment, it is also an error if AICs are installed which call for more than one programmable integrated function. This condition is detected in decision block 520 and if found an error is reported at error block 510. The process then ends at end block 515.

Page 12, Paragraph [0036].

[0036] It should be noted that embodiments are possible in which the system contains more than 1 fixed integrated function, for example J integrated functions, If so, decision block 505 would test for J integrated functions. It is also possible that the system contains more than 1 programmable function, for example K programmable functions. If so, decision block 510 would test for K programmable functions.

Page 15, Paragraph [0045].

[0045] The disclosed methodology allows multiple functions to connect to physical layers depending on what particular AIC is plugged into an industry standard PCIE connector or slot. A PCIE link is used to communicate a custom or standard PCIE protocol to an AIC compatible with the industry standard PCIE connector. The physical layer of an AIC is discovered and configuration of the various switches, MUXs and functions is completed prior to system boot. When a PCIE AIC using PCIE protocol is plugged into a PCIE connector, the PCIE protocol as passed directly through to a PC link ~~since~~ because the native PCIE protocol requires no translation. Translation services are provided to the non-PCIE protocols from non-PCIE AICs that are plugged into the PCIE connectors. In this manner both PCIE and non-PCIE AICs are accommodated in the same industry standard connector.